wherein the mass-transfer of copper is suppressed through said copper alloy.

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22. (Amended) A semiconductor device comprising:

a semiconductor substrate;

an insulation layer over said semiconductor substrate, and said insulation layer having a trench groove;

a barrier metal layer on a bottom and side walls of said trench groove; and

an electrically conductive layer provided in an interconnection layer on said barrier metal layer, and said interconnection layer filling said trench groove,

wherein said interconnection layer comprises a copper alloy which includes at least one of Ag, As, Bi, P, Sb, Si and Ti in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit to copper, so that said copper alloy is in a solid solution.

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30. (Amended) A semiconductor device comprising:

a semiconductor substrate;

an insulation layer over said semiconductor substrate, and said insulation layer having a trench groove;

a barrier metal layer on a bottom and side walls of said trench groove; and

an electrically conductive layer provided in an interconnection layer on said barrier metal layer, and said interconnection layer filling said trench groove,

wherein said interconnection layer comprises a copper alloy which includes at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1

cont.
All

percent by weight.

Please add the following new claims:

-- 57. (New) An electrically conductive layer comprising:

a copper alloy which includes at least one of As, Bi, P, Sb, Si and Ti at more than 0.2

percent by weight,

said copper alloy formed on a substrate of said semiconductor circuit.

58. (New) An electrically conductive layer comprising:

a copper alloy which includes at least one of Bi, P, Sb and Ti at not less than 0.1

percent by weight,

said copper alloy formed on a substrate of said semiconductor circuit.

59. (New) An electrically conductive layer comprising:

a copper alloy which includes at least one of Ag, As, Bi, P, Sb, Si and Ti in a range of

not less than 0.1 percent by weight to not more than a maximum solubility limit to copper, so

that said copper alloy is in a solid solution,

said copper alloy formed on a substrate of said semiconductor circuit.

60. (New) An electrically conductive layer comprising:

a copper alloy which includes at least one of Ag, As, Bi, P, Sb, Si and Ti at not less

than 0.1 percent by weight and at least one of Mo, Ta and W in a range of not less than 0.1

percent by weight to not more than 1 percent by weight,

wherein said copper alloy has a melting point less than copper and the mass-transfer

of copper is suppressed through said copper alloy.

61. (New) An electrically conductive layer provided in a semiconductor circuit comprising:

a copper alloy which includes at least one of Ag, As, Bi, P, Sb, Si and Ti at not less

than 0.1 percent by weight,

said copper alloy provided in a groove within an inter-layer formed on a substrate of

said semiconductor circuit.

62. (New) The electrically conductive layer provided in a semiconductor circuit according to

claim 61, wherein said groove has a predetermined narrow width.

63. (New) The semiconductor device according to claim 22, wherein said trench groove has a

predetermined narrow width. - -

REMARKS

Applicant concurrently files herewith an excess claim fee for 3 independent claims.

Claims 1-37 and 57-63 are all claims presently pending in the application. Claims 38-

56 are respectfully canceled without prejudice or disclaimer. New claims 57 - 63 have been

added to more completely define the invention as well as new independent claim 60. Claims

1-37 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsuji et al. (U.S. Pat.

No. 5,004,520), Edelstein (U.S. Pat. No. 6,181,012 B1) and Dubin (U.S. Pat. No. 6,249,055

B1). These rejections are respectfully traversed in view of the following discussion.

Attached hereto is a marked-up version of the changes made to the specification